

## CLAIMS

1. A method for inspecting a mask, comprising:  
generating integrated circuit design data; and  
using information for interfeature relationships of the integrated circuit design data to inspect the mask.
2. The method of claim 1, wherein the interfeature relationships are on one layer of the integrated circuit design.
3. The method of claim 1, wherein the interfeature relationships are across multiple layers of the integrated circuit design.
4. The method of claim 1, wherein the interfeature relationships comprise:  
interfeature process proximity effects;  
interfeature coupling across layers;  
interfeature electronic relationships; or  
wire interconnects longer than a given length.
5. The method of claim 1, wherein the information for interfeature relationships includes information for identifying a redundancy of features, and using the information for interfeature relationships to inspect the mask further comprises:  
determining that at least one feature is functional; and  
waiving one or more defects on features redundant to the functional feature.
6. A method for performing metrology operations, including inspection, on a lithography photomask or wafer, comprising:  
generating integrated circuit design data; and  
using context information from the integrated circuit design data to inspect the photomask or wafer.

7. The method of claim 6, wherein using context information comprises:  
identifying to individual mask features or groups of mask features information relating to circuit elements intended to be produced from those mask features as defined in the integrated circuit design data.
8. The method of claim 6, wherein using context information comprises:  
analyzing mask features for contextual priority.
9. The method of claim 8, wherein using context information comprises:  
assigning priorities to all mask features or groups of mask features.
10. The method of claim 9, wherein assigning priorities to mask features comprises:  
applying criteria to mask design data by manual process.
11. The method of claim 9, wherein assigning priorities to mask features comprises:  
applying criteria to mask design data by computer-aided automated process.
12. The method of claim 6, wherein using context information comprises:  
analyzing integrated circuit design data for grouping in mask inspection areas.
13. The method of claim 6, wherein using context information comprises passing context information to a mask inspection system.
14. The method of claim 6, wherein the context information comprises information for neighboring geometries, electrical intent of the features, timing of the intended circuit, redundant features, and relationships of a given feature to neighboring features.
15. A method for mask inspection, comprising:  
designing an integrated circuit, wherein design data from the integrated circuit design comprises polygonal shape, location, layout geography, circuit functionality and circuit criticality data for each mask element;

- passing the design data to a context and priority analysis step;
  - analyzing design data for each mask element, wherein the analysis comprises comparing design data for each mask element to design data for other mask elements and to a predetermined set of mask criteria in order to determine a circuit function and circuit criticality context and priority for each mask element;
  - determining mask areas with similar resolution and analysis requirements;
  - including the circuit function and circuit criticality context and priority data and mask area data in a mask design data file; and
  - using the mask design data file to inspect a mask.
16. The method of claim 15, wherein analyzing design data comprises analyzing information for neighboring geometries, electrical intent of the mask elements, timing of the intended circuit, redundant mask elements, and relationships of a given mask element to neighboring mask elements.
17. The method of claim 15, further comprising ordering the mask design data file to enable efficient access to the data.
18. The method of claim 15, wherein determining comprises comparing the design data for adjacent mask elements and determining similarities.
19. A system for inspecting lithography masks, comprising:
- means for designing an integrated circuit, wherein design data from the integrated circuit design comprises polygonal shape, location, layout geography, circuit functionality and circuit criticality data for each mask element;
  - means for passing the design data to a context and priority analysis step; means for analyzing design data for each mask element, wherein the analysis comprises comparing design data for each mask element to design data for other mask elements and to a predetermined set of mask criteria in order to determine a circuit function and circuit criticality context and priority for each mask element;

means for determining mask areas with similar resolution and analysis requirements;

means for including the circuit function and circuit criticality context and priority data and mask area data in a mask design data file; and

means for using the mask design data file to inspect a mask.

20. The system of claim 19, wherein said means for analyzing design data comprises means for analyzing information for neighboring geometries, electrical intent of the mask elements, timing of the intended circuit, redundant mask elements, and relationships of a given mask element to neighboring mask elements.

21. The system of claim 19, further comprising means for ordering the mask design data file to enable efficient access to the data.

22. The system of claim 19, wherein said means for determining comprises means for comparing the design data for adjacent mask elements and determining similarities.

23. A system for inspecting a mask, comprising:  
means for generating integrated circuit design data; and  
means for using information for interfeature relationships of the integrated circuit design data to inspect the mask.

24. The system of claim 23, wherein the interfeature relationships are on one layer of the integrated circuit design.

25. The system of claim 23, wherein the interfeature relationships are across multiple layers of the integrated circuit design.

26. The system of claim 23, wherein the interfeature relationships comprise:  
interfeature process proximity effects;  
interfeature coupling across layers;

interfeature electronic relationships; or  
wire interconnects longer than a given length.

27. The system of claim 23, wherein the information for interfeature relationships includes information for identifying a redundancy of features, and said means for using the information for interfeature relationships to inspect the mask further comprises:
- means for determining that at least one feature is functional; and
  - means for waiving one or more defects on features redundant to the functional feature.
28. A system for performing metrology operations, including inspection, on a lithography photomask or wafer, comprising:
- means for generating integrated circuit design data; and
  - means for using context information from the integrated circuit design data to inspect the photomask or wafer.
29. The system of claim 28, wherein said means for using context information comprises:
- means for identifying to individual mask features or groups of mask features information relating to circuit elements intended to be produced from those mask features as defined in the integrated circuit design data.
30. The system of claim 28, wherein said means for using context information comprises:
- means for analyzing mask features for contextual priority.
31. The system of claim 30, wherein said means for using context information comprises:
- means for assigning priorities to all mask features or groups of mask features.
32. The system of claim 31, wherein assigning priorities to mask features comprises:
- applying criteria to mask design data by manual process.
33. The system of claim 32, wherein said means for assigning priorities to mask features comprises:

means for applying criteria to mask design data by computer-aided automated process.

34. The system of claim 28, wherein said means for using context information comprises:  
means for analyzing integrated circuit design data for grouping in mask inspection areas.

35. The system of claim 28, wherein said means for using context information comprises passing context information to a mask inspection system.

36. The system of claim 28, wherein the context information comprises information for neighboring geometries, electrical intent of the features, timing of the intended circuit, redundant features, and relationships of a given feature to neighboring features.

37. A method comprising:  
writing a mask;  
identifying an element of the mask having a potential mask defect;  
determining a relationship between geometry and function of the element; and  
determining if the potential mask defect is critical by using the relationship between geometry and function of the element.

38. The method of claim 38 wherein the relationship is determined by process modeling.

39. The method of claim 38 wherein the relationship is determined by device modeling.

40. The method of claim 38 wherein the relationship is determined by electrical modeling.

41. A system comprising:  
means for writing a mask;  
means for identifying an element of the mask having a potential mask defect;  
means for determining a relationship between geometry and function of the element; and

means for determining if the potential mask defect is critical by using the relationship between geometry and function of the element.

- 42. The system of claim 41 wherein the relationship is determined by process modeling.
- 43. The system of claim 41 wherein the relationship is determined by device modeling.
- 44. The system of claim 41 wherein the relationship is determined by electrical modeling.